REMARKS

Claims 1-4 are pending. Claim 1, the only independent claim, has been amended. The specification has been amended to correct a typographical error without adding new matter.

Claim 1 was objected to due to an informality. The amendment to claim 1 obviates that objection, in the manner proposed by the Examiner. Withdrawal of the objection is respectfully requested.

Claims 1-4 were rejected under 35 U.S.C. § 102(b) as anticipated by Tamura (EP 0 640 916 A2). Applicant submits that claim 1 is patentable over Tamura for at least the following reasons.

Claim 1 is directed to a computer system comprising a CPU for operating with pipe-line processing, a ROM storing a program to be executed by the CPU, and at least one ROM correction unit including a first storage unit for storing a subject address of an original instruction group in the program having a bug therein, a second storage unit for storing a modified instruction group for replacing the original instruction group by the modified instruction group having a branch address, a comparator for comparing a current address of a current instruction read from the ROM against the subject address, a selector for selecting the current address or the branch address based on a result of the comparison by the comparator, a flag generator for setting a ROM correction flag when the selector selects the branch address. The ROM correction unit delivers the ROM correction flag through a data bus (e.g., bus 56 in Figure 2).

As a result of the claimed structure, the CPU can judge the operation of the ROM correction unit based on the ROM correction flag delivered through a data bus.

In contrast, the output of the latch circuit in Tamura is not delivered through a data bus to the CPU, as a result of which the CPU cannot judge whether or not the latch circuit operated. Tamura's invention is directed to a fetch stage of pipe-line processing and

not to an execution stage of such processing. (See e.g., claim 3 of the present application, which specifies that the flag is set at an execution stage of a branch instruction.)

For at least the reasons discussed above, claim 1 is believed patentable over Tamura. Withdrawal of the rejection is requested.

The other claims in this application are each dependent from the independent claim discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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